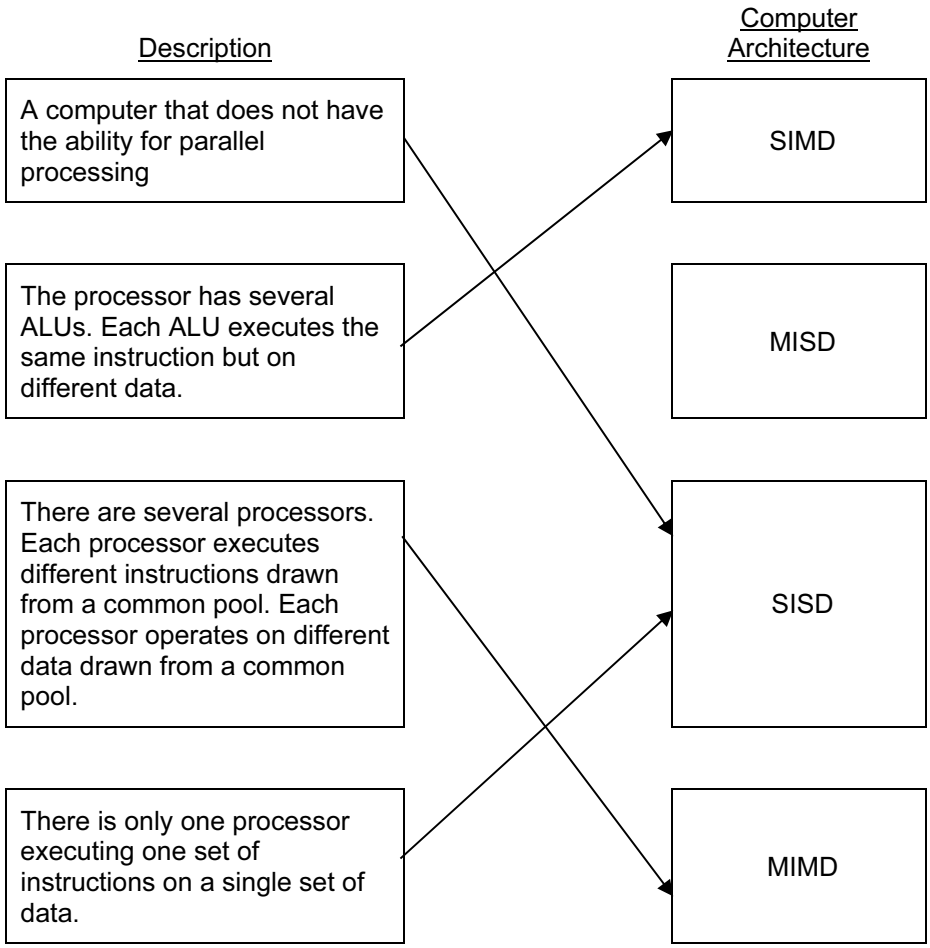
QUESTION 1.

4 **(a)** 1 mark for correct arrow from each description



[4]

(b) **(i)** **Massive**: many/large number of processors // hundreds/thousands of processors [1]

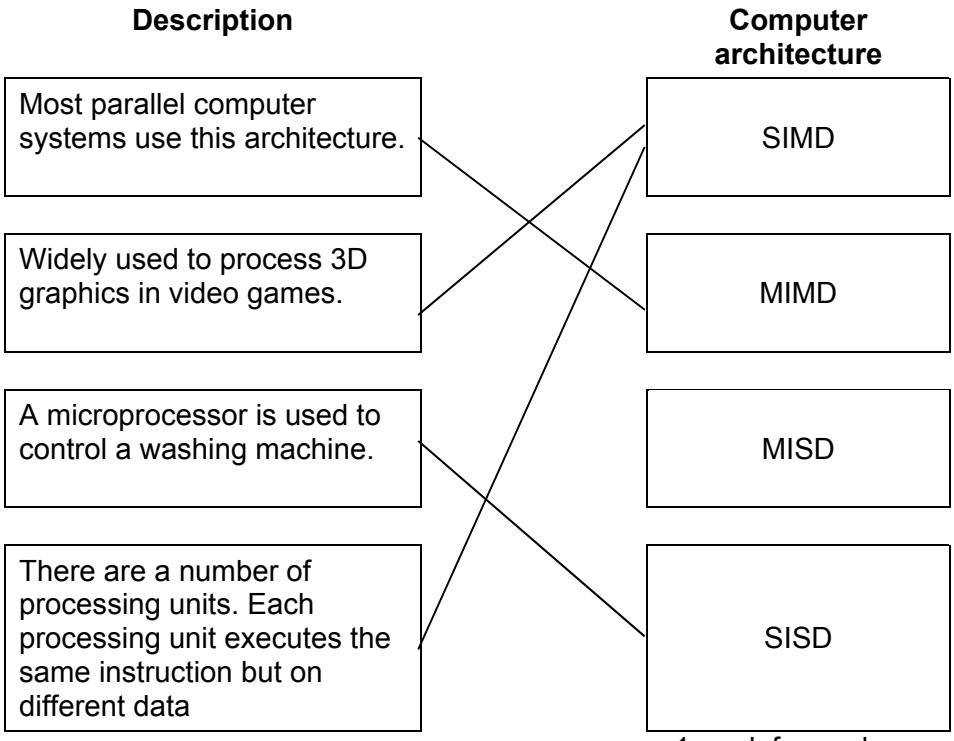
(ii) **Parallel**: to perform a set of coordinated computations in parallel/simultaneously [1]

(c) processors need to be able to communicate … [1]
so that processed data can be transferred from one processor to another [1]

suitable algorithm/program/software/design // appropriate programming language [1]
which allows data to be processed by multiple processors simultaneously [1]

[Total: 10]

QUESTION 2.

Question	Answer	
2(a)	 1 mark for each correct line	
2(b)	• Only one (separate) processor / not many separate processors (is not massively parallel) 1 • Quad core computer system // processing units share the same bus 1 **1 mark** for each point, **max 2**	**2**
2(c)	• Split into blocks of code …. • … that can be processed simultaneously … • … instead of sequentially • Each block is processed by a different processor • which allows each of the many processors to simultaneously process the different blocks of code independently • Requires both parallelism and co-ordination **1 mark** for each point, **max 2**	**2**
2(d)	**1 mark** for identification of hardware issue, for example: • Communication between the different processors is the issue **1 mark** for further explanation from: • Each processor needs a link to every other processor • Many processors require many of these links • Challenging topology	**2**

QUESTION 3.

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>5(a)</td><td>1 mark per bullet point to max 4:
• RISC has fewer instructions // CISC has more instructions
• RISC has many registers // CISC has few registers
• RISCs instructions are simpler // CISC's instructions are more complex
• RISC has a few instruction formats // CISC has many instruction formats
• RISC usually uses single-cycle instructions // CISC uses multi-cycle instructions
• RISC uses fixed-length instructions // CISC uses variable-length instructions
• RISC has better pipelineability // CISC has poorer pipelineability
• RISC requires less complex circuits // CISC requires more complex circuits
• RISC has fewer addressing modes // CISC has more addressing modes
• RISC makes more use of RAM // CISC makes more use of cache/less use of RAM
• RISC has a hard-wired control unit // CISC has a programmable control unit
• RISC only uses load and store instructions to address memory
// CISC has many types of instructions to address memory</td><td>4</td></tr>
<tr><td>5(b)(i)</td><td>1 mark per bullet point:
• Completing the As correctly
• B in column 2, row 1 no other Bs in row 1
• Remainder correctly completed

<table>
<tr><th rowspan="2">Stage</th><th colspan="9">Time interval</th></tr>
<tr><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th></tr>
<tr><td>Fetch instruction</td><td>A</td><td>B</td><td>C</td><td>D</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Decode instruction</td><td></td><td>A</td><td>B</td><td>C</td><td>D</td><td></td><td></td><td></td><td></td></tr>
<tr><td>Execute instruction</td><td></td><td></td><td>A</td><td>B</td><td>C</td><td>D</td><td></td><td></td><td></td></tr>
<tr><td>Access operand in memory</td><td></td><td></td><td></td><td>A</td><td>B</td><td>C</td><td>D</td><td></td><td></td></tr>
<tr><td>Write result to register</td><td></td><td></td><td></td><td></td><td>A</td><td>B</td><td>C</td><td>D</td><td></td></tr>
</table></td><td>3</td></tr>
</table>

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>5(b)(ii)</td><td>1 mark per bullet point:
• Correct number of cycles for pipelining 8
• Correct number of cycles without pipelining 4 × 5 = 20
• No of cycles saved 20 – 8 = 12</td><td>3</td></tr>
<tr><td>5(c)</td><td>1 mark for each row
<table><tr><th rowspan="2">Statement</th><th colspan="3">Architecture</th></tr><tr><th>SIMD</th><th>MIMD</th><th>SISD</th></tr><tr><td>Each processor executes a different instruction</td><td></td><td>✓</td><td></td></tr><tr><td>There is only one processor</td><td></td><td></td><td>✓</td></tr><tr><td>Each processor executes the same instruction input using data available in the dedicated memory</td><td>✓</td><td></td><td></td></tr><tr><td>Each processor typically has its own partition within a shared memory</td><td></td><td>✓</td><td></td></tr></table></td><td>4</td></tr>
</table>

QUESTION 4.

<table>
<tr><th>Question</th><th>Answer</th><th></th></tr>
<tr><td>7(a)</td><td>1 mark for 2/3 rows correct
2 marks for 4/5 rows correct
3 marks for 6 correct rows

<table><tr><th>Statement</th><th>RISC</th><th>CISC</th></tr><tr><td>Larger instruction set</td><td></td><td>✓</td></tr><tr><td>Variable length instructions</td><td></td><td>✓</td></tr><tr><td>Smaller number of instruction formats</td><td>✓</td><td></td></tr><tr><td>Pipelining is easier</td><td>✓</td><td></td></tr><tr><td>Microprogrammed control unit</td><td></td><td>✓</td></tr><tr><td>Multi-cycle instructions</td><td></td><td>✓</td></tr></table></td><td></td></tr>
<tr><td>7(b)(i)</td><td>1 mark per bullet point

• SISD // Single instruction single data
• SIMD // Single instruction multiple data
• MISD // Multiple instruction single data
• MIMD // Multiple instruction multiple data</td><td>4</td></tr>
<tr><td>7(b)(ii)</td><td>1 mark per bullet point (max 3)

• Large number of processors
• … working collaboratively on the same program
• … working together simultaneously on the same program
• … communicating via a messaging interface</td><td>3</td></tr>
</table>

QUESTION 5.

<table>
<tr><th>Question</th><th>Answer</th><th></th></tr>
<tr><td>9(a)</td><td>1 mark for each correct term

<table>
<tr><th>Description</th><th>Term</th></tr>
<tr><td>• There are several processors.
• Each processor executes different sets of instructions on one set of data at the same time.</td><td>MISD</td></tr>
<tr><td>• The processor has several ALUs.
• Each ALU executes the same set of instructions on different sets of data at the same time.</td><td>SIMD</td></tr>
<tr><td>• There is only one processor.
• The processor executes one set of instructions on one set of data.</td><td>SISD</td></tr>
<tr><td>• There are several processors.
• Each processor executes a different set of instructions.
• Each processor operates on different sets of data.</td><td>MIMD</td></tr>
</table>
</td><td></td></tr>
<tr><td>9(b)</td><td>1 mark per bullet point to max 3

• A large number of processors
• Collaborative processing // coordinated simultaneous processing
• Network infrastructure
• Communicate using a message interface / by sending messages</td><td>3</td></tr>
</table>